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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/877,037	06/11/2001	Takao Ishida	401251	9811

23548 7590 07/22/2004

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EXAMINER	
JONES, STEPHEN E	

ART UNIT	PAPER NUMBER
2817	

DATE MAILED: 07/22/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/877,037	ISHIDA ET AL.	
	Examiner	Art Unit	
	Stephen E. Jones	2817	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *04 May 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *13-16* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *13-16* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Applicant's arguments, see the appellant's appeal brief, filed 5/4/04, with respect to claims 13-16 have been fully considered and are persuasive. The finality of the office action dated 1/14/04 has been withdrawn.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

4. Claims 15-16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hosoya (of record) in view of Microwave Semiconductor Circuit Basis and Application (ISBN4-526-03386-3).

Hosoya (Fig. 16) teaches an MMIC circuit including: a transistor (1) having a MIM capacitor (18) (i.e. metal insulator metal) connected to the output line of the transistor,

and a bias circuit (17) is connected in parallel to the MIM Capacitor (Claim 16), and an open stub capacitance (12) is provided for matching the impedance. Furthermore, it is an inherent property that the capacitance of a MIM changes inversely with the thickness of its insulating film. Also, when one is describing impedance matching it is understood that all possible impedance mismatches are considered and thus impedance variations in the output capacitance of the transistor and the MIM capacitor due to variations in the thickness of their insulating film would be part of the impedance matching (i.e. compensated for).

However, Hosoya does not explicitly teach that the MMIC transistor has the same insulating layer as the MIM capacitor.

Microwave Semiconductor Circuit Basis and Application provides an exemplary teaching of how an MMIC transistor and a MIM capacitor can be connected in which the insulation layer is shared (see Fig. 5.16).

It would have been considered obvious to one of ordinary skill in the art to have connected the transistor and MIM capacitor such that they share the insulation layer such as taught by "Microwave Semiconductor Circuit Basis and Application" in the Hosoya device, especially since Hosoya is silent as to the structure of the connection and it would have been considered a well-known art-recognized equivalent/alternative means for constructing the MMIC device.

5. Claims 13-14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hosoya (of record) in view Microwave Semiconductor Circuit Basis and Application (ISBN4-526-03386-3) and Okada (of record).

Hosoya teaches an MMIC with output matching as described above. However, Hosoya does not explicitly teach an input matching circuit or that the MMIC transistor has the same insulating layer as the MIM capacitor (18) on the input side.

Okada (Fig. 19, along with Figs. 6B and 13B) teaches using similar matching circuits for both the input and output of a transistor (see Col. 13, lines 10-15).

Microwave Semiconductor Circuit Basis and Application provides an exemplary teaching of how an MMIC transistor and a MIM capacitor can be connected in which the insulation layer is shared (see Fig. 5.16).

It would have been considered obvious to one of ordinary skill in the art to have included similar matching circuits (such as taught by Okada) for the input and output of the Hosoya circuit such that both the input and output have stub matching circuits, because it would have provided the advantageous benefit of impedance matching not only the output but also the input, thereby suggesting the obviousness of such a modification.

Furthermore, it would have been considered obvious to one of ordinary skill in the art to have connected the transistor and MIM capacitor such that they share the insulation layer such as taught by "Microwave Semiconductor Circuit Basis and Application" in the Hosoya/Okada device, especially since Hosoya is silent as to the

structure of the connection and it would have been considered a well-known art-recognized equivalent/alternative means for constructing the MMIC device.

Response to Arguments

Applicant's arguments with respect to the rejections using Hosoya alone and Hosoya in view of Okada are convincing since Hosoya does not explicitly teach that the insulation layers of the MMIC transistor and the MIM capacitor are the same. However, Hosoya does teach a connection between the transistor and capacitor. One of ordinary skill in the art would find it obvious to obtain such a connection structure from what is known in the art. Thus the new rejections using the "Microwave Semiconductor Circuit Basis and Application" reference with Hosoya and Okada have been applied as described above.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Stephen E. Jones whose telephone number is 571-272-1762. The examiner can normally be reached on Monday through Friday from 8 AM to 4 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Robert J. Pascal can be reached on 571-272-1769. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Stephen Jones
Patent Examiner
Art Unit 2817

SEJ